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Description

Configuration for the digital-analog conversion of a high-frequency
5 digital input signal into a carrier-frequency analog output signal

The invention relates to a configuration for the digital-analog conversion of a high-frequency digital input signal into a carrier-frequency analog output signal according to the preamble to Claim 1.

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Architectures for the generation of a broadband, carrier-frequency output signal are known in which, in a low frequency range, a digital input signal is converted into an analog signal using a digital-analog converter, and then reconverted into the carrier-frequency output signal using one or more mixing stages.

Furthermore, digital-analog converter architectures are known in which a carrier-frequency output signal is generated from a high-frequency digital input signal without further frequency conversion.

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The carrier-frequency analog output signal in this case also has unwanted carrier frequencies in addition to a desired carrier frequency. These unwanted carrier frequencies can be caused, for example, by a less than perfect digital input signal or by various unwanted modulation mechanisms.

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In the described architectures, cost-intensive filters with high quality or mixers with high linearity, which are always configured on the output end and which must be adjusted to a required carrier frequency range in each case, are necessary. These must be replaced, 30 at great expense, if a change in carrier frequency range is required.

The paper "1-MHz and 16-bit $\Sigma\Delta$ DAC with a 224th order reconstruction FIR filter using only 9 nonzero taps", by Jansson and Svensson, 35 published in the Proceedings of the 7th Annual IEEE International ASIC Conference and Exhibit, Rochester, NY, USA, 19-23 September 1994, XP 010140531, pages 29-32, ISBN 0-7803-2020-4, discloses a

configuration for digital-analog conversion in which an input signal arrives both directly, and also sometimes with a number of time delays, at current sources arranged in parallel to one another. This 5 configuration has a FIR filter structure which is determined by defined filter coefficients c_1, \dots, c_{224} .

US 5,323,157 A discloses a sigma-delta digital-analog converter, in which an "input data" signal is interpolated and oversampled and fed 10 to a sigma-delta modulator with a clock frequency MCLK. The sigma-delta modulator forms a signal A_{out} , which is fed to a series circuit comprising a plurality of D-type flip-flops. Each inverse output of a D-type flip-flop under consideration is connected both to a D-type flip-flop connected subsequently in series in the serial 15 circuit, and to a current source. The current sources are combined on the output side to form an analog output signal V_{out} .

The object of this invention is therefore to design a configuration 20 for digital-analog conversion in such a way that it can be adjusted to various carrier frequency ranges without great cost.

The object of this invention is achieved by the features described in Claim 1. Advantageous developments of the invention are described 25 in the subclaims.

30 The configuration for digital-analog conversion according to the invention has an integrated filter characteristic, thus eliminating the need for cost-intensive mixers or filters at the output end.

35 It consists of a plurality of D/A converters configured parallel to one another, whereby specific coefficients are assigned to each of the individual D/A converters. This enables the configuration to be ideally adjusted to a required carrier frequency range.

40 The configuration according to the invention can be adjusted to different carrier frequency ranges by modifying the clock frequency of the D/A converters accordingly.

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According to the invention, it is particularly preferable for a FIR filter characteristic to be realized and/or integrated into the configuration through the selection of the coefficients that are 5 specifically assigned to the D/A converters and of the delay times that are specifically assigned to the delay elements. The consecutive coefficients correspond to a sampling of an impulse response from a filter that has a required filter characteristic. In this way the carrier-frequency output signal has a higher spectral 10 purity compared to a form implemented without filter characteristic.

Claims

1. Configuration for the digital-analog conversion of a high-frequency digital input signal (DE) into a carrier-frequency analog output signal (AA),
 - 5 - in which a delay device (VZ) has at least one first delay element (VG1) and additional delay elements (VG2, ..., VGn) connected downstream from the first in a serially consecutive manner,
 - 10 - in which the digital input signal (DE) is connected to an input of the first delay element (VG1) and is connected to an input of a first D/A converter (W0),
 - in which the first delay element (VG1) is connected on the output side to an input of another D/A converter (W1) assigned thereto, and, optionally, each additional delay element (VG2, ..., VGn) is connected on the output side to an input of another D/A converter (W2, ..., Wn) assigned to the respective delay element (VG2, ..., VGn),
 - 15 - in which all D/A converters (W0, ..., Wn) controlled with an identical clock signal (CLK) are combined on the output side in a step-by-step manner so that output signals (AS0, ..., ASn) of all D/A converters (W0, ..., Wn) form the analog output signal (AA), and
 - in which a specific coefficient (k0, ..., kn) is assigned to each 20 D/A converter (W0, ..., Wn) and a specific delay time (τ1, ..., τn) is assigned to each delay element (VG2, ..., VGn) for the purpose of realizing a filter characteristic,
characterized in that
 - the delay times (τ1, ..., τn) specifically assigned to the delay 25 elements (VG1, ..., VGn) correspond to an entire clock period or to part of the clock period of the clock signal (CLK), and in that
 - the clock signal (CLK) is selected such that the filter characteristic is automatically adjusted if there is a change in carrier frequency range of the output signal.

2. Configuration according to one of the above claims, in which the specific coefficients (k_0, \dots, k_n) and the specific delay times (τ_1, \dots, τ_n) are selected such that a FIR filter characteristic is realized.

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3. Configuration according to one of the above claims, in which the delay elements (VG_1, \dots, VG_n) are configured as D latches timed with the clock signal (CLK).

10 4. Configuration according to one of the above claims, in which the D/A converters (W_0, \dots, W_n) are configured as 1-bit D/A converters.

15 5. Configuration according to one of the above claims, in which the D/A converters (W_0, \dots, W_n) are combined on the output side by means of adding devices (AE_1, \dots, AE_n).

20 6. Configuration according to one of the above claims, in which the delay times (τ_1, \dots, τ_n) assigned to the delay elements (VG_1, \dots, VG_n) are identical.

25 7. Configuration according to one of the above claims, in which the output signals (AS_0, \dots, AS_n) of the D/A converters (W_0, \dots, W_n) each have a multiple pulse sequence in order to improve the filter function.

8. Configuration according to one of the above claims, in which the digital input signal (DE) is broadband.

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